DESIGN OF A PHASE LOCKED LOOP AS A FREQUENCY MULTIPLIER USING SELF HEALING CIRCUIT

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Abstract— High performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. The circuit performance are degraded by some factors such as variability, leakage and improper matching in the device. when this particular PLL is made in the CMOS technology, it will lead to some leakage and variability. This paper proposes the PLL design as a frequency multiplier using self-healing circuit that will detect the fault and compensate the condition. we use self-healing prescalar and self-healing VCO by Bottom level detector and Current compensator for the correct functioning. The complete design is done in PROTEUS software and checked.

Keyword: PLL, Self healing, prescalar/VCO, Charge pump, Loop filter.

I.INTRODUCTION

The basic block diagram of a PLL is shown in Figure. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock, CKref, to produce a high frequency clock, CKout.

The operation of a PLL is as follows. The phase detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. The difference or error

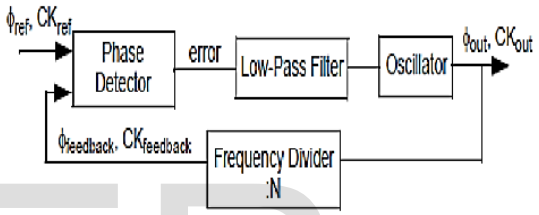

Fig 1 Basic PLL Block Diagram

signal is low-pass filtered and drives the oscillator. The filtered error signal acts as a control signal (voltage or current) of the oscillator and adjusts the frequency of oscillation to align φfeedback with φref. The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock has a constant phase error and the same frequency as the reference clock. Because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference clock.

A phase-locked loop (PLL) is widely employed in wireline and wireless communication systems. The poor device matching and leakage current vary the common-mode voltage of a ring-based voltage-controlled oscillator (VCO) over a wide frequency range. It may limit the oscillation frequency range of a VCO and causes a VCO not to oscillate in a worst case. To realize a wide-range PLL, the divider following aVCO should operate between the highest and lowest frequencies.When a PLL works at a higher

frequency which the static circuits cannot operate, dynamic circuits are needed.
A true-single-phase-clocking (TSPC) divider is widely used to realize a prescaler for this PLL. A TSPC prescaler must work over a wide frequency range to cover the process and temperature variations. For a TSPC prescaler, the undesired leakage currents may limit its frequency range or alter the original states of the floating nodes to have a malfunction.
The leakage current and current mismatch in a charge pump (CP) will degrade the reference spur and jitter significantly. To mitigate the above problems, a self-healing divide-by-4/5 prescaler and a self-healing VCO are presented in this paper. A time-to-digital converter (TDC) and a 4-bit encoder are used to quantize the phase error and digitally calibrate the CP. This paper is organized as follows. Section II describes the block description. Section III describes the circuit functioning. Section IV concludes the proposel. Section V shows the result and progress.

II. BLOCK DESCRIPTION

A. Phase Frequency Detector:

The phase frequency detector, PFD, measures the difference in phase between the reference and feedback signals. If there is a phase difference between the two signals, it generates up or down synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an up signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage $V_{control}$. On the contrary, if the error signal from the PFD is a downsignal, the charge pump removes charge from the LPF capacitor, which decreases $V_{control}$.$V_{control}$ is the input to the VCO. Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an upsignal, the VCO speeds up. On the contrary, if a down signal is generated, the VCO slows down. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, thus creating a closed loop frequency control system.

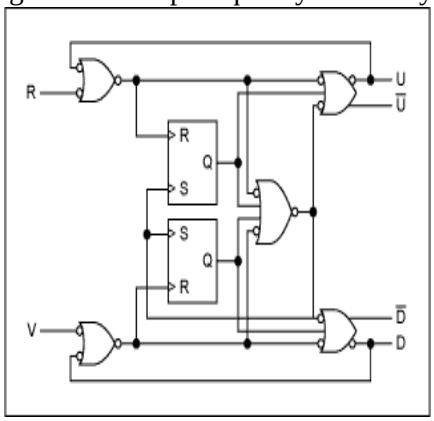

Fig 2: Phase Frequency Detector Circuit

B.Charge Pump:

A charge pump is a kind of DC to DC converter that uses capacitors as energy storage elements to create either a higher or lower voltage power source. Charge pump circuits are capable of high efficiencies, sometimes as high as 90–95% while being electrically simple circuits.

The term 'charge pump' is also used in phase-locked loop (PLL) circuits. This is a completely different application. In a PLL the phase difference between the reference signal (often from a crystal oscillator) and the output signal is translated into two signals UP and DN. The two signals control switches to steer current into or out of a capacitor, causing the voltage across the capacitor to increase or decrease. In each cycle, the time during which the switch is turned on is proportional to the phase difference, hence the charge delivered is dependent on the phase difference also. The voltage on the capacitor is used to tune a voltage-controlled oscillator (VCO), generating the desired output signal frequency. The use of a charge pump naturally adds a pole at the origin in the loop transfer function of the PLL, since the charge-pump current is driven into a capacitor to generate a voltage (V=I/(sC)). The additional pole at the origin is desirable because when considering the closed-loop transfer function of the PLL, this pole at the origin integrates the error signal and causes the system to track the input with one

more order. The charge pump in a PLL design is constructed in integrated-circuit (IC) technology, consisting of pull-up, pull-down transistors and on-chip capacitors. A resistor is also added to stabilize the closed-loop PLL.

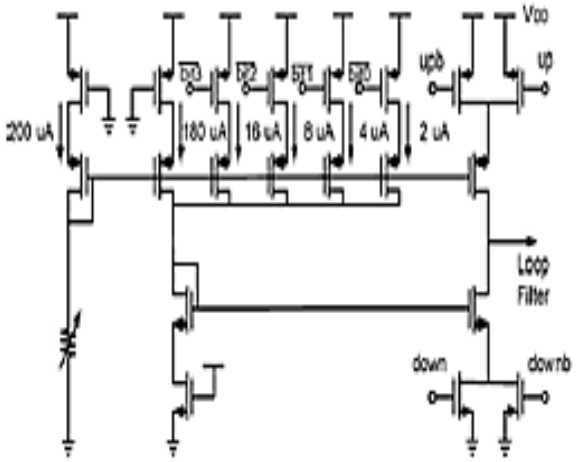

Fig 3: Digitally Controlled Charge Pump

C.Voltage Controlled Oscillator:

self-healing VCO is realized by four gain stages, a bottom level detector, and a current compensator,a gain stage. This gain stage consists of a differential amplifier with active loads and a cross-coupled pair with digitally-controlled current sources.

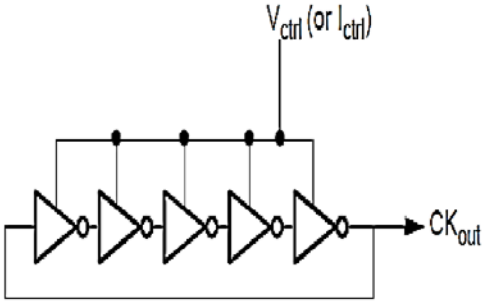

Fig 4: Five Stage Ring Oscillator

The leakage current is much smaller than that a minimum-size MOS can provide. These circuits have been simulated and verified for all corners and a supply voltage variation of 10% at the temperature of C C. Similarly, when a malfunction is detected, the compensators will turn on M7B or M7C to a variable resistor controlled by .The cross-coupled pair,and , enhances the output swing of this VCO. The output common-mode voltage and the output swing of the VCO are altered by the leakage currents, the total tail currents, and the resistances of and . They are dependent upon the process variations. For example, when the resistances of and are decreased, the oscillation frequency of this VCO is increased. It will result in the output swing decreased and the bottom level is increased. It also leads to a limited oscillation frequency range.

If a larger biasing current and the cross-coupled pair with larger dimensions are selected for this VCO, the output swing can be increased. However, it may waste the power when the operation frequency of this PLL is low. In this work, the self-healing VCO using a bottom-level detector can achieve a wide tuning range and low power.

The bottom-level detector is shown in the VCO's output swing. A self-biased buffer enlarges the output of a VCO into a rail-to-rail swing. So, the output,of this self-biased buffer and have the same polarity.When goes high and is high, the NOR gate will enable and disable , respectively.

The current of the transistor will charge the capacitor, , to increase When goes low and is low, two cases will be discussed.If the bottom level of is larger than the comparator's output goes high and the NOR gate goes low to enable and disable , respectively. The transistor will charge the capacitor,to increase . For the other case, if the bottom level of is lower than the comparator's output goes low and the NOR gate goes high to disable and enable respectively. The transistor will discharge the capacitor to decrease .In the steady state, the voltage on the capacitor, will track the bottom level of the VCO's swing. For the current compensator, a reference voltage represents the target bottom level of the VCO's swing and it is compared with by a comparator. When the VCO's bottom level is smaller than the target one or the output common-mode voltage of this VCO is high enough.Then, the output of the comparator goes high and enables Q1. The current compensator enables the auxiliary tail current to lower the output common-mode voltage. Then, it reduces the VCO's bottom level to be lower than . If the above case is not

true, Q2 will be enabled and turn on the auxiliary tail current . It further lowers the VCO's bottom level.

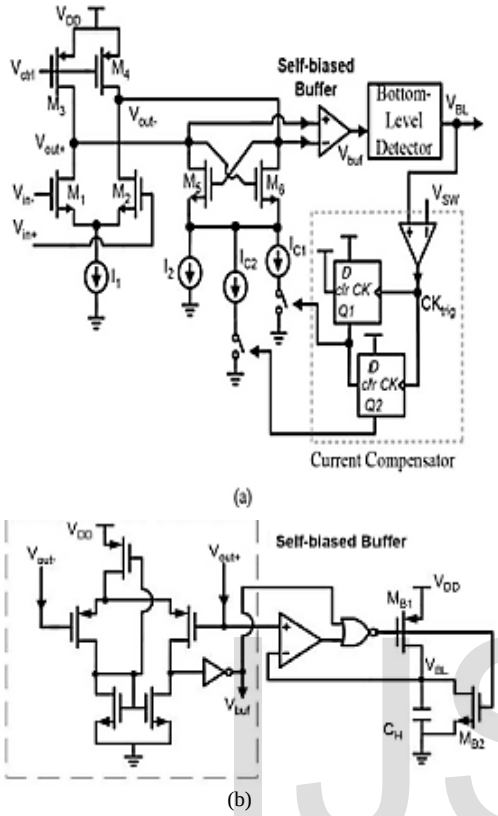

Fig:5(a) Current Compensator & Bottom Level Detector 5(b) Bottom Level Detector Circuit.

D. Dual Modulus Prescaler:

Prescalers are typically used at very high frequency to extend the upper frequency range of frequency counters, phase locked loop (PLL) synthesizers, and other counting circuits. When used in conjunction with a PLL, a prescaler introduces a normally undesired change in the relationship between the frequency step size and phase detector comparison frequency. For this reason, it is common to either restrict the integer to a low value, or use a dual-modulus prescaler in this application. A dual-modulus prescaler is one that has the ability to selectively divide the input frequency by one of two (normally consecutive) integers, such as 32 and 33. Common fixed-integer microwave prescalers are available in modulus 2, 4, 8, 5 and 10, and can operate at frequencies in excess of 10 GHz.

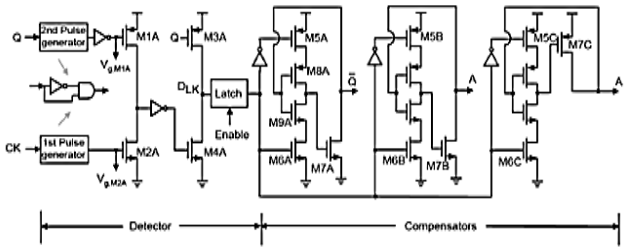

Fig:6(a) prescaler circuit 6(b) self healing dual modulus prescaler circuit

III.CIRCUIT FUNCTIONING

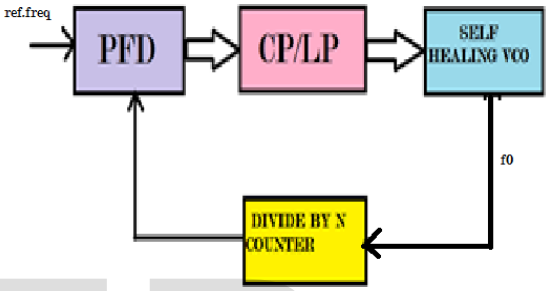

Fig:7 Proposed PLL Block Diagram

The above block diagram shows the proposed PLL design in which the phase frequency detector detects the frequency difference between the reference input to the obtained output frequency. The output of the PFD is fed to the charge pump/loop filter circuit, which accounts for the non linear performance of the circuit. It is being shown and simulated for the performance below. The obtained output from LP is fed to the self healing VCO that detects and compensates the leakage that occurs.The self healing prescalar and the counter output is given back as a feedback to the PFD.

IV.CONCLUSION

Self-healing technique is being added to the VCO and the Prescaler functioning inorder to overcome the leakage and variability. It is designed and simulated for correctness. Due to additional active devices, the jitter performance of a self healing PLL will be degraded, compared to a PLL without a self-healing technique.

V. RESULT AND PROGRESS

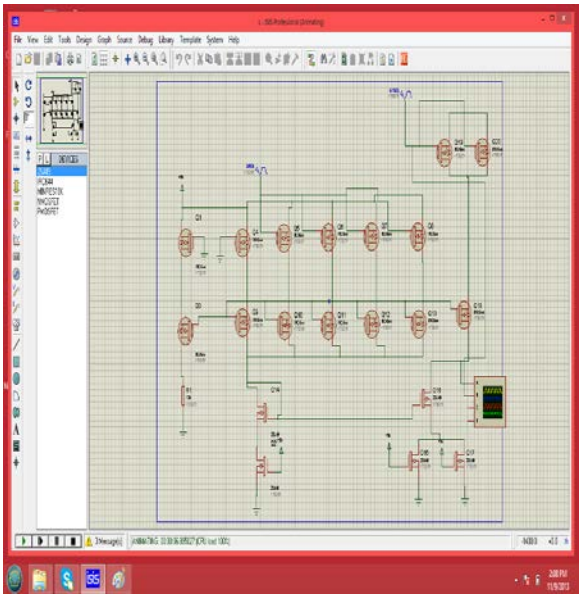

Fig:8 Schematic Design

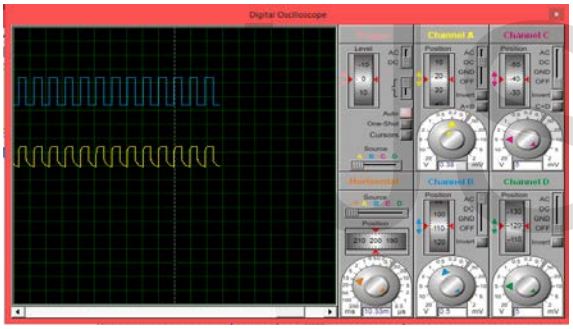

Fig:8(a) Showing the Leakage

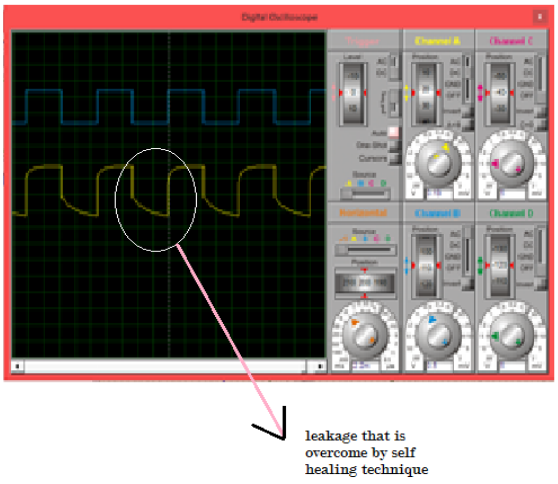

Fig: 8(b) Self Healing Technique Usage

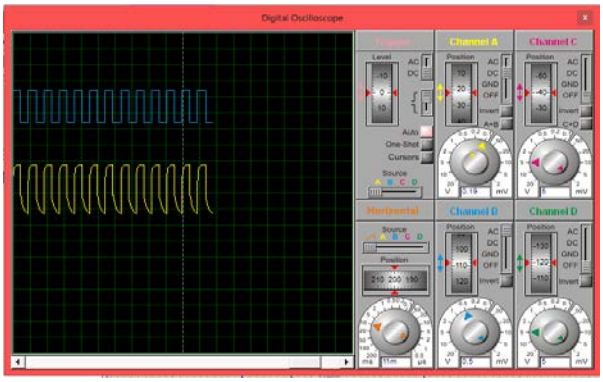

Fig:8(c) Waveform With Varying Amplitude And Time Period

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